APPENDIX B

VERSION WITH MARKINGS TO SHOW CHANGES MADE
37 C.F.R. § 1.121(b)(iii) AND (c)(ii)

SPECIFICATION:

Paragraph beginning at page 5, line 24 to page 6, line 3:

According to this aspect of the invention, the gate electrode may be silicon dioxide and may have a thickness which is less than 1000Å. The N-type channel region may be formed by a 100 KeV phosphorus implant at a dose of between [5.5E13] $5.5x10^{13}$ atoms/cm^2 and [8.0E13] $8.0x10^{13}$ atoms/cm^2. The gate electrode may have a doping concentration roughly corresponding to a 50 KeV boron implant dose of [5E15] $5x10^{15}$ atoms/cm^2.

Paragraph beginning at page 6, line 7:

According to this aspect of the invention, the gate oxide may be formed by a pyrogenic process. The gate oxide may be annealed after its formation and may have a thickness of about 500 to 1000Å. The N-type channel region may be formed by a phosphorus implant at a dose of about [7.0E13] $7.0x10^{13}$ atoms/cm^2.

Paragraph beginning at page 9, line 10:

After the openings 32 and 33 have been formed, a phosphorus ion implant is carried out in which ions are implanted through the openings 32 and 33 to form shallow N+ regions 34 and 35, respectively. The ion implant step is carried out at an energy of approximately 120 KeV at a dose of about [3.0E15] $3.0x10^{15}$ atoms/cm^2, for example.

Paragraph beginning at page 9, line 16:

Thereafter, a second mask is applied, and a further oxide etch is carried out in which a part of the remaining portion of oxide layer 31 is removed from the active areas of the chip but is

left in the termination regions (not shown). A boron ion implant step is then carried out at an energy of roughly 120 KeV and at a dose of about [1E12] $1x10^{12}$ atoms/cm^2, for example. The boron implant reduces the JFET resistance and forms an enhanced P- layer 36, shown in Figure 3. A screening oxide layer may be grown in the device areas prior to the enhancement implant.

Paragraph beginning at page 10, line 15:

The etched areas 40 and 41 serve as openings for subsequent channel and source implants which are shown in Figure 7. Typically, a phosphorus ion implant step is carried out at a dose of roughly [5.5E13] $5.5x10^{13}$ atoms/cm^2 to [8E13] $8x10^{13}$ atoms/cm^2 and at an energy of about 100 KeV, for example. A screening oxide may be grown prior to the implant to protect the surface of the wafer. The phosphorus ions are then driven in to form regions 42 and 43 having a desired junction depth.

Paragraph beginning at page 10, line 24 to page 11, line 2:

Then, boron ions are implanted through openings 40 and 41. The implant is typically carried out at an energy of about 50 KeV at a dose of approximately [3E15] $3x10^{15}$ atoms/cm^2, for example, and is then driven in to form the P+ source regions 44 and 45 shown in Figure 8.

Paragraph beginning at page 11, line 26 to page 12, line 11:

Following the formation of the gate oxide layer 46, a polysilicon layer 47 is formed over the device surface and, in accordance with another aspect of the invention, is heavily doped with boron. A blanket dose of boron is implanted into the polysilicon to form a layer of P-type polysilicon from which the gate electrode is subsequently formed, according to this aspect of the invention. The polysilicon is doped with about a [5E15] $5x10^{15}$ atoms/cm^2 dose at an energy of roughly 50 KeV, for example. The polysilicon layer 47 is then covered by a very shallow oxide layer (not shown) which can have a thickness, for example, of about 500Å and can serve as a mask for patterning the polysilicon layer 46 in a later step.

Paragraph beginning at page 12, line 26 to page 13, line 7:

The interlayer oxide 50 is then doped with approximately a [1E14] $1x10^{14}$ atoms/cm^2 dose of arsenic ions at an energy of about 120 KeV, for example. The arsenic implant changes the etch rate of the doped portion of the interlayer oxide 50 so that during the subsequent etching steps, the oxide is etched to have tapered profiles 53 and 54 in the contact area. This tapered profile improves the step coverage of the subsequently deposited contact metal layer.

Paragraph beginning at page 17, line 11 to page 18, line 3:

Here, the caps of the T0-3 packages were removed, and the devices placed into a vacuum chamber. An ion beam was directed onto the die and covered the complete die surface. The samples were irradiated, one at a time, for a period determined by the ion flux and the desired fluence of the ion beam. In this example, the ion flux was limited to [1E4] $1x10^4$ ions/cm^2/s and the fluence was set at [5E5] $5x10^5$ ions. In this example, the samples were irradiated with krypton ions with an LET of 41 MeV/(mg/cm^2) at an energy of four hundred MeV. Devices of each high power type were tested at each combination of Vgs and Vds bias. The measured threshold voltages of each device are shown in Figure 14. As shown, the threshold voltage remains with the -5V specification. Thus, the P- channel device of the invention is suitable for both total radiation dose environments as well as SEE environments, particularly for the more common applications where the P- channel device receives a positive gate voltage of no more than a few volts.

CLAIMS:

1. (Amended) A MOS gated device which is resistant to single event radiation failure and having improved total dose radiation resistance; said device comprising:

a P-type substrate having substantially flat, parallel upper and lower surfaces;

a plurality of laterally spaced N-type body regions extending from said upper surface into said substrate;